1 Introduction

We try to estimate the consumption of the Very Front End board of the SPD, overall and for each of the supplied voltages.

2 Supplied voltages

Besides the photomultiplier high voltage, 5 different voltages are supplied to the VFE board:

- Analog +1.65 ASIC polarisation $V_{cc}$, threshold references $V_{refH} - V_{refL}$ and DACs.
- Analog -1.65 ASIC polarisation $V_{ce}$.
- Digital +1.65 ASIC digital part, FPGA.
- Digital -1.65 ASIC digital part FPGA.
- Analog 3.3 Subtractor reference, subtractor bias $V_{BiasH}$, $V_{BiasL}$, OpAmps, Pull Ups.
- Digital 3.3 LVDS multiplexers.

3 Analog +1.65

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Measured</th>
<th>Current (mA) per channel</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{cc}$</td>
<td></td>
<td>20</td>
</tr>
<tr>
<td>$V_{refH} - V_{refL}$</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>DACs and references</td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>

Overall 22 mA per channel. For all 64 channels, 1408 mA. These data are directly measured on the ASIC. Measures have been performed on RUN4 ASIC.

4 Analog -1.65

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Measured</th>
<th>Current (mA) per channel</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{ce}$</td>
<td></td>
<td>20</td>
</tr>
</tbody>
</table>

Overall 20 mA per channel. For all 64 channels, 1280 mA.
5 Digital +1.65

- measured Clock Division 40 mA
- measured ASIC Digital parts 1 mA per channel
- estimation FPGA 500 mA

For all 64 channels and one clock divider 604 mA.

6 Digital -1.65

- measured Clock Division 40 mA
- measured ASIC Digital parts 1 mA per channel
- estimation FPGA 500 mA

For all 64 channels and one clock divider 604 mA.

7 Analog +3.3

- measured Subtractor reference 1 mA per channel
- measured $V_{BiasH}$ 0.5 mA per channel
- measured $V_{BiasL}$ 0.5 mA per channel
- measured OpAmps 1 mA per channel
- measured Pull Ups 1 mA per channel

Overall 4 mA per channel, for 64 channels 256 mA

8 Digital +3.3

data sheet LVDS multiplexers 75 mA per multiplexer

Overall, for 64 channels and 4 multiplexers, 300 mA.

9 Radiation Hard Regulators

Radiation Hard regulators are capable of delivering up to 3A current. Leaving a safety margin consisting in delivering around 1.5 A per regulator, we should count for:

- 1 analog +1.65 regulator per board. 100 in total.
- 1 analog -1.65 regulator per board. 100 in total.
- 1 analog +3.3 regulator every 5 boards. 20 in total.
- 1 digital +1.65 regulator every 2 boards. 50 in total.
- 1 digital -1.65 regulator every 2 boards. 50 in total.
- 1 digital +3.3 regulator every 5 boards. 20 in total.

Overall we estimate to need 190 positive regulators and 120 negative ones. We have ordered 200 positive regulators and 175 negative regulators.
10 Power consumption

After the quoted currents, the estimated total power consumption is

Analog ±1.65 4.5 W.
Digital ±1.65 2 W.
Analog 3.3 0.85 W.
Digital 3.3 1 W.

In total 8.3-8.5 W.

11 Not taken into account

The following items have not been taken into account in this estimation.

- Drivers, buffers and converters